Amorphous-Silicon Thin-Film Transistor with Two-Step Exposure Process

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ABSTRACT

The two-step-exposure (TSE) technology has been developed in application for combination the active layer with metal II layer. And this TSE technology has been applied in our Reduced-Mask process (five-mask) for cost reduction. The result shows that this amorphous-silicon thin-film transistor with four-photolithography process has great potential in mass production.

Keywords: Two-step exposure technology, a-Si thin-film transistor

1. INTRODUCTION

Amorphous-silicon thin-film transistor displays have already entered the market and are used in notebook PC, desktop type monitor and so on. As far as the a-Si TFT manufactures are concerned, there are two factors to keep them in a better position for competition. One is the process yield another is the process cost. At present, mass production for a-Si thin film transistors (TFT) usually take six or seven (even more) photolithography processes [1-5]. It's believed that reduction of the photolithography process will put it in a better position for competition.

The a-Si TFT process flow of the conventional six-mask BCE (back-channel-etched) type is Metal I (gate electrode), Island (active layer), Contact, ITO, Metal II (source/drain electrode), Passivation. In ERSO, we have already developed the Reduced Mask (five-mask) process. Its process flow is Metal I (gate electrode), Island (active layer)/Metal Mask, Metal II (source/drain electrode), Passivation, ITO. Based on this experiment, we developed the ***two-step-exposure*** **(TSE)** technology to combine Island layer with MII layer in one photolithography process. In this paper, we will discuss the TSE technology and the TFT characteristic of this a-Si TFT with four-photolithography process.

2. EXPERIMENT

TFT's were fabricated with the combination of standard BCE type Reduced Mask (5-mask) process and **TSE** technology. This four- photolithography process flow is listed as below, **Figure 1** shows the schematic diagram of our TFT pixel. **1:** MoW was sputtered and patterned as gate electrode. **2:** SiNx (gate insulator), intrinsic a-Si, n+ a-Si were deposited and Cr/ Al/Cr were sputtered as the MII source-drain electrode. Following is the **two-step-exposure** (**TSE**) process, the photoresist was coated and exposed pattern A with higher light intensity—complete exposure (**Figure 2**), exposed pattern B with lower intensity —incomplete exposure (**Figure 3**). Then developed the TSE pattern, so there was still some photoresist on pattern B (channel region). The next step, MII wet etching and n+ a-Si, a-Si, SiNx dry etching. After patterning TSE pattern, the photoresist on pattern B (channel region) was etched with O2 plasma ashing. Because the photoresist on pattern B was thinner than that on the other region, the photoresist on pattern B could be etched completely and remain about 7000～8000 Å thickness on the other part if O2 plasma ashing uniformity、rate/time were well controlled. Next, MII on the channel region was wet etched and then stripped off the photoresist. Then used MII as the mask to dry etch n+ a-Si. ***3:*** Passivation layers. ***4:*** ITO layer. Step 3and 4 were completed by using conventional 5-mask Top ITO process method.

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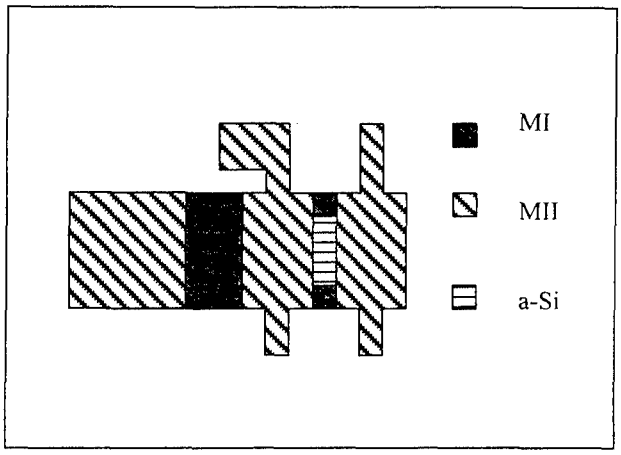
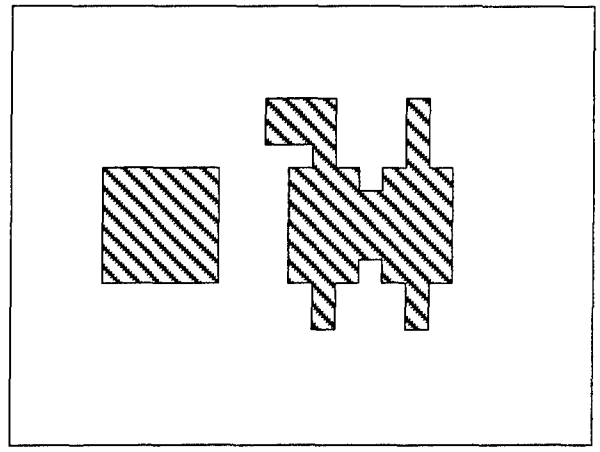


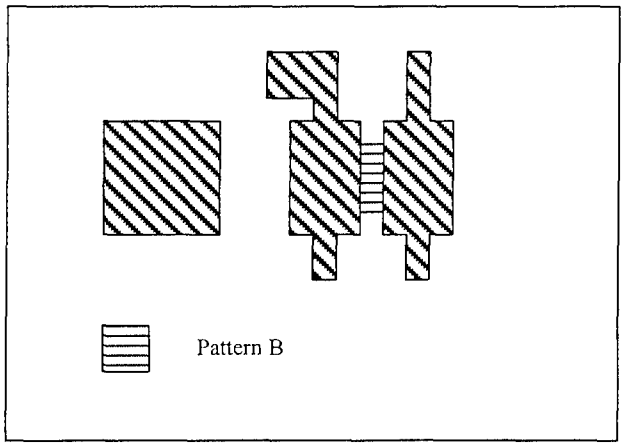
TFT pixel top view

Figure 1



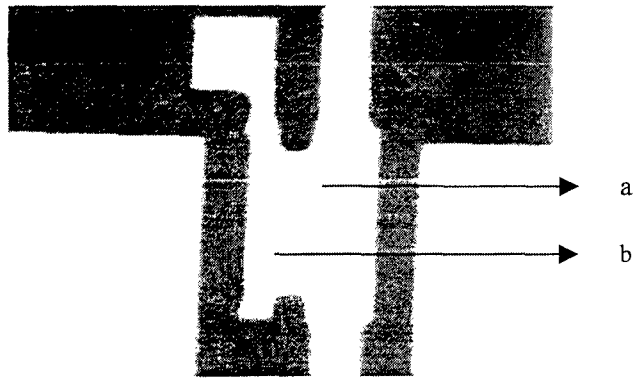
TSE pattern A

Figure 2



TSE pattern B

Figure 3



Photograph of TFT pixel top view

Figure 4

3. PROCESS CHARACTERISTIC

It is considered there are two critical steps in this four-photolithography process. One is TSE process another is O2 plasma ashing.

3.1. Two-Step-Exposure (TSE) Process

The general issues in this process are the photoresist thickness and thickness uniformity of pattern B. Those are not easy to control because the photoresist of not being completely developed usually creates a large deviation on thickness. Besides, if the photoresist thickness difference between pattern A and pattern B (incomplete exposure) is not larger than 3000 Å, there will be a very narrow process window in the O2 plasma ashing and the n+a-Si etching. Furthermore, photoresist pattern of incomplete exposure usually produces very dull edge. In **Figure 4** there is the dull edge in point A and B. If the edge is too smooth, the PR of these side walls will connect on the top and bottom area of the channel region. This will cause some residue in following channel MII etching process and fail in n+a-Si etching.

The effect of the etching process on photoresist thickness is another factor that should be considered. In island etching process (after first MII wet etching) photoresist was etched about 300 Å and O2 plasma etching rate was about 3000Å. Because of this two etching factor, the photoresist thickness on the channel region can't be too thin. In other words, increase the photoresist thickness will widen the process window.

In this study, we coated 1.5 μm SHIPLEY photoresist and tried many exposure intensity. The best condition we've found was listed as below: Eth of complete exposure is 70mj/cm2, Eth of incomplete exposure is 35mj/cm2 and remained photoresist with the thickness of 8000 Å$\sim$9000 Å in the channel region. The thickness of photoresist remained in the channel region is very safe for the following n+ a-Si /a-Si dry etching and O2 etching process.

3.2. O2 plasma ashing

In this work, two mode of O2 plasma ashing process were studied: PE mode and RIE mode. **Table 1** shows the etching recipe of two different etchers that we used. When using RIE mode O2 plasma ashing to remove photoresist on the channel region, the following MII wet etching failed. The MII on the channel region could not be removed by wet etching even with a long period of overetching which only produced serious lateral etching, and led to source-drain MII broken. By using PE mode O2 plasma ashing to remove photoresist on the channel region, no process issue of this kind was occurred. The cause of this process issue might be the surface of the top MII layer Cr formed CrOx in RIE mode O2 plasma ashing process and this is reasonable. In PE mode, chemical reaction dominates the etching process, and less energy (momentum) will be transfer to the film. There for, it's harder to surmount activation energy to form CrOx.

Cl2 plasma treatment before MII wet etching is one method that we've tried to solved this issue. It was effective but the uniformity was not easy to control. In addition, change the MII material or etch the channel MII with dry etching process may be another solution to this issue.

RF mode	RIE	PE
O2 (sccm)	400	400
power(W)	800	500
cooler temp	20	40
pressure(m Torr)	100	375
result	MII residue	no residue

Table 1

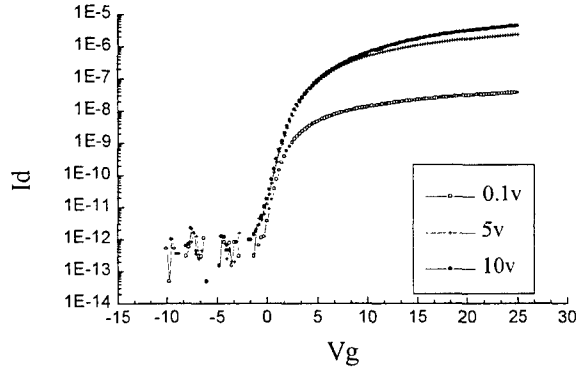


FIGURE 5

4. TFT CHARACTERISTIC

The drain-source current Ids vs. the gate-source voltage Vgs characteristic at room temperature is plotted in **Figure 5.** The threshold voltage Vth is about 2.63 v, field effect mobility μ_{FE} is about 0.74 cm2/v-sec, subthreshold swing is about 0.72v/dec. The result shows that the TFT characteristic won't be obviously affected by the series etching process.

5. SUMMARY

In general, the process issue of TFT mass production line partly comes from the photoresist residue or particle contamination, which will cause the MII open or MI/MII short. To advance MII process earlier can reduce the probability of such occurrence. And this is the spirit of the a-Si TFT array with four-photolithography process. Besides, this process also has the characteristic of island metal masking structure [6], which can protect the active layer from plasma damage in plasma etching process. In addition to the benefits of process reduction and those listed above, better contact condition between MII and island layer is also another benefit of this process.
Studies in this paper conclude that four-photolithography a-Si TFT is highly potential in mass production.

6. REFERENCE

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